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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,005	12/12/2000	Kazuyuki Ito	NEC 444	3384

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Norman P. Soloway
HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C.
175 Canal Street
Manchester, NH 03101

EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/735,005	Applicant(s) ITO, KAZUYUKI
	Examiner Samuel A Gebremariam	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 5, line 24 "layer 102" is a misrepresentation of layer "202" of fig. 3C. Also on line 25 of page 5, there are no gate patterns G1 and G2 in neither figs. 3 and 4. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "forming a trench in said semiconductor substrate" is not clear as to where the trench is formed with respect to other elements of the device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37 and 39-41, are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Gilbert US patent No. 5,885,856.

Regarding claim 37 admitted prior art teaches (figs. 3A-3C and 4) a method for manufacturing a semiconductor device comprising the steps of: forming a conductive layer (202) over the semiconductor substrate (201) forming a photoresist pattern layer on the conductive layer using a photomask having gate patterns (P1) and (P2) corresponding to the active areas and dummy gate patterns (DP) corresponding to the dummy areas and patterning the conductive layer by an etching process using the photoresist pattern.

Admitted prior art does not disclose forming a first photoresist pattern layer, a first photomask and forming a trench in the semiconductor substrate by an etching process using the first photoresist pattern layer.

It is conventional and well known to form isolation trench using photolithographic process. Gilbert also teaches (fig. 1, col. 2, lines 41-60) forming isolation trench (13) using masking layer (12) between active areas (14) and dummy regions (20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first masking process for forming trench isolation trench structure taught by Gilbert in the process of admitted prior art in order to form isolation structures between the active region before forming the gate and dummy gate structures.

Regarding claims 39 and 40 admitted prior art teaches substantially the entire claimed method of claim 37 above except explicitly stating that the dummy areas and or dummy gates are arranged in at least two rows and/ or two columns and the row is

shifted from another and the row and/ or at least one column is shifted from another column.

It is conventional and also taught by Gilbert (fig. 6 and 7) arranging device structures in an array as claimed.

It would well within ordinary skill in the art to arrange the dummy gate and gate structures of admitted prior art device in the conventional manner in order to obtain high packing density.

Regarding claim 41 admitted prior art teaches substantially the entire claimed method of claim 37 including forming a plurality of dummy active areas and a plurality dummy gates on the dummy active areas (figs. 3A-3C).

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Gilbert and in further view of Shimomura et al. US patent No. 6,140,687.

Regarding claim 38 admitted prior art teaches substantially the entire claimed method of claim 37 above except explicitly stating that the shape of the dummy area and/ or dummy gate is a circle.

It is conventional and also taught by Shimomura forming circular shaped gates.

It would be well within ordinary skill in the art to select circular shape dummy/gate structures since circular structures allow for symmetrical arrangement of integrated circuit layout. Furthermore since it is known to form circular shaped gate electrodes it would have been obvious to form circular dummy gate electrode.

Respons to Arguments

4. Applicant's arguments with respect to claims 37-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
February 10, 2003

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800